

INFORMATION DISCLOSURE CITATION				<i>Complete If Known</i>	
				Application Number	10/763,849
				Filing Date	January 22, 2004
				First Named Inventor	Mark A. Horowitz
				Art Unit	2181 2111
				Examiner Name	To be assigned Anvt
				Attorney Docket Number	60809-5000
Serial No.	Date	Office	of	1	

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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Examiner Initials	Foreign Patent Document Country Code ² - Number ³ - Kind Code ⁴ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Translation	
						Yes	No
						X	
						X	
						X	

OTHER NON-PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
<i>MA</i>	GABARA, THADDEUS J., "Digitally Adjustable Resistors in CMOS for High-Performance Applications", <i>IEEE J. Solid-State Circuits</i> , vol. 27, no. 8, August 1992.

Examiner Signature	I-PA/3519923.1 	Date Considered	9/7/2003
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INFORMATION DISCLOSURE CITATION PTO-1449				<i>Complete If Known</i>		
Sheet	1	of	2	Application Number	To be assigned 10/763849	
				Filing Date	January 22, 2004	
				First Named Inventor	Mark A. Horowitz et al.	
				Art Unit	2181 2101	
				Examiner Name	Auve, Glenn Allen	
				Attorney Docket Number	60809-5000	

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Examiner Initials	Document Number Number - Kind Code ¹	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Filing Date if Appropriate
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Examiner Signature	Glen Auve	Date Considered	9/7/2003
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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MA	Intel, "82243BX Host Bridge Datasheet", pp. 2-4, 3-25 to 3-27, 4-19 to 4-20		
MA	Intel, "Intel® 440BX AGPset: 82443BX Host Bridge/Controller:Datasheet", TOC: pp. 1-1 to 5-9 (1998)		
MA	Poulton, "Signaling in High-Performance Memory Systems", ISSCC, 1-59 (1999)		
MA	Song and Soo, "NRZ Timing Recovery Technique for Band-Limited Channels", IEEE Journal of Solid-State Circuits, 32(4):514-520 (1997)		

Examiner Signature	Glenn Auve	Date Considered	9/7/2003
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<p style="text-align: center;">INFORMATION DISCLOSURE CITATION</p> <p style="text-align: center;">MAY 11 2005</p> <p style="text-align: center;">PTO-1449</p> <p style="text-align: center;">1 of 1</p>				Complete If Known			
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/MA		6,661,268	12-09-2003	Stark et al.	327	170	
/MA		6,516,365	02-04-2003	Horowitz et al.	710	104	
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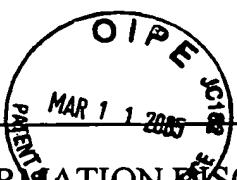
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/MA		Intel Corporation, "Intel 430 TX PCISET: 82439 TX System Controller (MTXC)", February 1997.					
/MA		NAKASE et al., "Source Synchronization and Timing Vernier Techniques for 1.2-GB/s SDRAM Interface", IEEE J. Solid-State Circuits, vol. 34, No. 4, April 1999.					
/MA		PARIS et al., "WP 24.3: An 800 MB/s 72 Mb SDRAM with Digitally-Calibrated DLL", ISSCC Slide Supplement, IEEE, 1999.					
/MA		SLDRAM Inc., "400/Mb/s/pin", July 9, 1998.					

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1-PA/3543115.



INFORMATION DISCLOSURE CHARTER

PTO-1449

Sheet

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**Examiner
Signature**

Glenne Ave

Date
Considered

9/7/2003

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1-PA/3536161.J